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(71) Applicant *(for all designated States except US)*: DSC COMMUNICATIONS A/S [DK/DK]; Lautrupbjerg 7–11, DK–2750 Ballerup (DK).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: JØRGENSEN, Morten [DK/DK]; Vedelev Bygade 53, DK–4000 Roskilde (DK).

(74) Agent: HOFMAN–BANG & BOUTARD, LEHMANN & REE A/S; Hans Bekkevolds Allé 7, DK–2900 Hellerup (DK).

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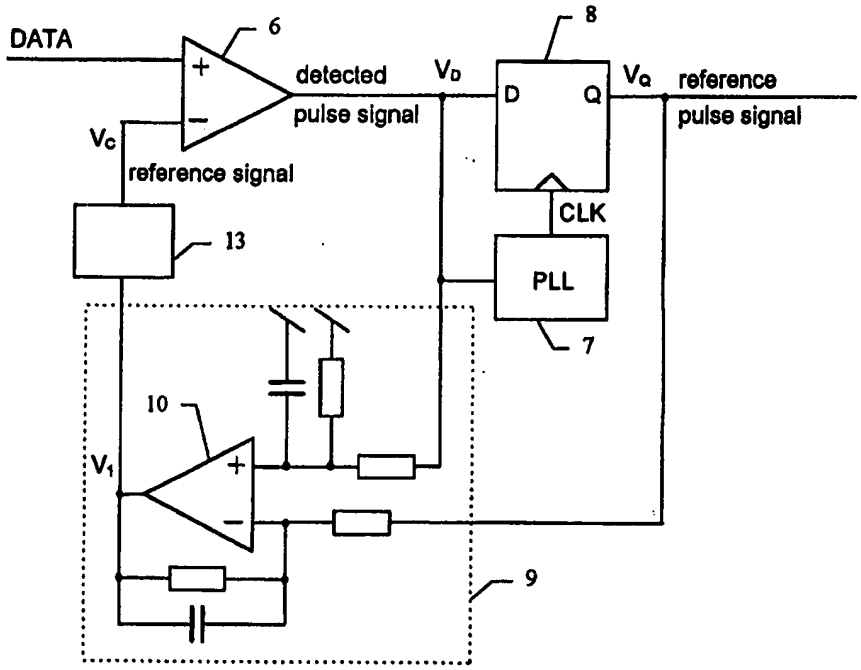
(54) Title: A METHOD OF DETECTING PULSE–SHAPED DATA SIGNALS AND A CIRCUIT FOR PERFORMING THE METHOD

(57) Abstract

When a signal having inclined flanks, e.g. as a result of a transmission of the signal, is detected, varying pulse widths will occur depending on the signal composition of logic 0's and 1's. These varying pulse widths are a problem when setup and holding times for a detection circuit are to be observed. The invention provides a signal having more ideal pulse widths, also even if the logic 0's and 1's are distributed dissimilarly. The DATA signal is detected by means of a comparator (6) to generate the detected pulse signal V_D, which is sampled by means of the circuit (8) controlled by the clock extraction circuit (7). This results in the reference pulse signal V_Q, and a reference signal for the comparator (6) is generated by means of the circuit (9) so that the pulse width of V_D is approximately equal to the pulse width of V_Q.



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A method of detecting pulse-shaped data signals and a circuit for performing the method

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The invention relates to a method of detecting pulse-shaped data signals, wherein the data signals are compared with a reference signal, which is dependent on the data signals, to generate a detected signal.

It is well-known that e.g. logic circuits have a certain setup time and holding time for the circuit to respond to an input signal. When a data signal is to be detected, it is therefore important that the detection takes place at such a point in the data pulse that both sufficient setup-time and holding time are available. Data signals to be detected usually differ from their ideal shape. For example, a data signal representing logic 1 may be too wide with respect to the clock period which represents the frequency of the data signal, and this will give rise to interference with the detection of the data signal.

It is well-known to detect a data signal by comparison with a reference signal by means of a comparator to which a reference signal is fed. The reference signal may e.g. be generated as a mean value of the received data signals, or, as described in German Offenlegungsschrift DE 38 16 973 A1, be generated as a difference between signals which represents the detected signal and an inverted version of the detected data signal, respectively. If 1's and 0's are distributed fairly equally in the data signal, this prior art may give a reasonable compensation for the mentioned pulse width variations. However, in case of a too great imbalance between the number of 1's and the number of 0's in the data signal the prior art will cause the detected pulse width to be wrong and the reference signal to be moved out into the outer range of

the amplitude of the signals where the signal/noise ratio is relatively small, thereby involving the risk of error detection.

The object of the invention is to provide a method which gives a better compensation of pulse width variations than has been possible in the past, and wherein this compensation works even in case of imbalance between the number of 1's and the number of 0's in the data signal.

This object is achieved by extracting a clock signal from the detected signal to generate a reference pulse signal in response to the detected pulse signal, and comparing the detected pulse signal and the reference pulse signal to generate the reference signal so that the pulse width of the detected pulse signal is adjusted to correspond to the reference pulse width.

The reference pulse width corresponds to a whole clock period, which is well-defined with respect to the data signal frequency, and the method of the invention thus ensures that the detected pulse signal is generated with an approximately correct pulse width, which is in turn due to the best conditions for maximum setup time and holding time in connection with the detection.

The reference signal is adjusted with a certain attenuation in accordance with the type of data signals which are transmitted, and the control signal preferably varies slowly with respect to the frequency of the data signals.

If the data signal pulses differ much from the ideal shape, the reference signal may be relatively close to the maximum and minimum values of the data pulses, and it may therefore be expedient to limit the range within which the reference signal may be adjusted.

In practice, it may be expedient to make comparisons on the basis of differential signals, as differences in the DC levels from the various circuits may easily occur.

The invention also concerns a circuit for performing the method according to claim 1 and of type which is defined in the introductory portion of claim 5. The circuit is characterized in that it comprises a clock extraction circuit adapted to generate a clock signal from the detected pulse signal, and comprises a generator circuit adapted to generate a reference pulse signal representing the detected pulse signal with a pulse width which is dependent on the clock signal period, as well as comprises a comparison circuit adapted to compare the detected pulse signal with the reference pulse signal to generate the reference signal so that the pulse width of the detected pulse signal is adjusted to correspond to the reference pulse width.

Preferably, the generator is a D-flip-flop adapted to receive the detected pulse signal on the data input and to receive the generated clock signal on the clock input.

A preferred embodiment of the comparison circuit is a differential amplifier whose inputs are connected to receive the detected pulse signal and the reference pulse signal, respectively.

Signal limitations may be introduced into the control loop in different ways, i.a. comprising low-pass filtering of the detected pulse signal and the reference pulse signal. Other forms of limitation may also be introduced into the actual reference signal e.g. in the form of maximum and minimum values.

A compensation circuit may be inserted with a view to compensating differences in the logic voltage levels. The compensation circuit may be in the form of one, preferably two differential amplifiers for the detected pulse signal and the reference pulse signal, respectively. In the event that just one differential circuit is used, this may be connected to one of the pulse signals (the detected pulse signal or the reference pulse signal), so that the output signal may be adjusted in terms of DC relative to the DC level of the other pulse signal.

The invention will now be described more fully with reference to the drawing, in which

fig. 1 shows a circuit for detecting data signals using prior art,

fig. 2 shows an embodiment of a circuit according to the invention for detecting data signals,

fig. 3 illustrates the temporal course of selected signals in connection with the detection of a data signal using a circuit according to the invention,

fig. 4 shows an example of a detection of a data signal using prior art and the technique according to the invention, respectively,

fig. 5 shows an embodiment of a circuit according to the invention in which a possible difference in logic voltage levels is compensated.

Fig. 1 shows an example of a circuit for detecting data signals using prior art. The circuit detects an arriving data signal DATA using a threshold value for a comparator, said threshold value being a mean value based on

maximum and minimum amplitude of DATA. It should be noted that the concepts threshold value and reference voltage have the same meaning in this context.

The data signal DATA is fed as a first input signal to a comparator 1. The data signal DATA is also fed to a reference signal generator 2 consisting of two diodes and an RC network. The output signal V_c from the reference signal generator 2 is fed as a second input signal to the comparator 1.

The comparator 1 forms an output signal V_D which is logic 1 when the data signal DATA is greater than the reference signal V_C, and which is logic zero when the signal DATA is smaller than the reference signal V_C.

The signal V_D is fed to a clock extraction circuit 3 which extracts the clock signal CLK with the frequency corresponding to the clock in the signal V_D. The clock extractor 3 may e.g. be built using a digital phase-locked circuit in a well-known manner.

The signal V_D is also fed to the data input on a D-flip-flop 4. The extracted clock signal CLK is used as a clock signal for the D-flip-flop 4. The output signal V_Q of the D-flip-flop will thus be a sampled signal with a clock period determined by the clock signal CLK.

As described, the data signal DATA will be detected by the circuit in fig. 1, but the circuit has the drawback that the pulse width of the output signal V_D will vary depending on the data signal DATA. The reason is that the data signal DATA will typically have inclined flanks, e.g. as a result of a low-pass filtering in connection with a transmission of the signal, and the threshold value will therefore affect the pulse width of the signal

V_D. The threshold value is determined by temporally averaging the data signal DATA in the reference signal generator 2 and will therefore vary when the signal DATA varies. For example, a single logic 1 among many logic 0's will cause a relatively low threshold value V_C to be generated, and this will have as a result that the pulse width of a detected pulse will be relatively wide owing to the inclined flanks of the pulse.

Fig. 2 shows an embodiment of a circuit for detecting data signals according to the invention. The circuit detects an arriving signal DATA and uses an adaptive reference signal for adjusting the pulse width of the detected pulse.

A data signal DATA is fed to a first input of a comparator 6 which is indicated as a simple comparator, but which may be implemented in various ways depending on the bit rate of the data signal DATA. For example, the comparator will be composed of high rate components when the data signal DATA has a high bit rate. The adaptive, determined reference signal V_C is fed to the second input of the comparator 6. The comparator 6 hereby forms a signal V_D which is logic one when the signal DATA is greater than the reference signal V_C, and which is logic zero when the signal DATA is smaller than the reference signal V_C.

The output signal V_D from the comparator 6 is fed to the clock extraction circuit 7 which extracts a clock signal CLK with a frequency equal to the clock frequency corresponding to the signal V_D. As mentioned before, the clock extraction circuit 7 may be implemented as a digital phase-locked circuit.

The signal V_D is fed to the data input of a D-flip-flop 8, and the clock signal CLK is fed to the clock input of the D-flip-flop 8. The signal V_D is hereby sampled by the D-flip-flop 8 at the times determined by the clock signal CLK, and the signal V_Q is generated.

The signals V_D and V_Q are fed to a differential low-pass filter 9 which generates the signal V_1. The differential low-pass filter 9 is based upon a differential amplifier 10. The signal V_1 is fed to a limiter unit 13 whose output signal V_C is used as a reference signal for the comparator 6. The limiter unit 13 limits the signal V_C so that overloading of the comparator 6 is avoided. The limiter unit may also be adapted to keep the reference signal within very narrow limits, so that the difference between DATA and the reference signal does not become too small.

The control loop adapts itself such that the temporal mean value of the signals V_D and V_Q is the same. As the pulse width of the output signal V_Q is determined by the clock signal CLK, the adjustment will thus mean that a threshold value V_C is used so that the pulse width is kept constant even though the DC component of the data signal DATA varies.

In the situation where the input signal V_D and the output signal V_Q from the D-flip-flop 8 have the same low and the same high logic voltage levels, the output value V_C of the differential amplifier which corresponds to the difference between the temporal mean values of the signals V_D and V_Q will also correspond to the difference between the pulse width of the signals V_D and V_Q. The circuit will therefore cause detection of the signal DATA using the adaptive threshold value V_C, so that the pulse width of the signal V_D is kept constant.

If, however, the input signal V_D and the output signal V_Q from the D-flip-flop 8 do not have the same low and same high logic voltage levels, the circuit must be extended to compensate for the difference in the logic voltage levels. It is illustrated in fig. 5 how this may be done. The desirability of adjusting the pulse width of the signal V_D so that it is equal to the period time of the clock signal CLK, may be ascribed inter alia to the temporal conditions which must be observed according to the specification for the D-flip-flop circuit 8 used. Thus, it is necessary to observe the given setup and holding time specifications for the signal applied to the data input to ensure that the D-flip-flop 8 operates correctly.

If, e.g., the signal DATA is detected so that the pulse width of the signal V_D is smaller than the period time of the clock signal CLK fed to the D-flip-flop 8, it may be difficult to observe the specified setup and holding times. Correspondingly, a data pulse width of the signal V_D greater than the period time of the clock signal CLK may make it difficult to observe the mentioned setup and holding times for the subsequent data pulses which are fed to the D-flip-flop 8. Thus, it is of interest to adjust the pulse width of the signal V_D so that it corresponds to the period time of the clock signal CLK, and, as mentioned, this is done by adjusting the threshold value V_C which is fed to the comparator 6.

Fig. 3 shows an example of the temporal course of the input signal DATA and the output signal V_D from the comparator 6 using the circuit shown in fig. 2. In the adjustment described in connection with fig. 2, the threshold value V_C will be adjusted currently so that the temporal mean value of the signal V_D is equal to the temporal mean value of the output signal V_Q.

It is illustrated in the upper portion of fig. 3 how the threshold value V_C is adjusted from having the value Th1 to later having the value Th2. The change in the threshold value V_C is a result of the adjustment to ensure that the pulse width of the data signal DATA measured at the level of the reference signal corresponds to the pulse width of the clock signal CLK, i.e. that V_D has the same temporal mean value as the output signal V_Q.

Fig. 4 shows an example of a detection of a data signal using prior art and the technique of the invention, respectively. It is illustrated in fig. 4(a) how the detection takes place using the prior art, in which the threshold value V_C is determined as a temporal mean value of the data signal DATA. Thus, using the threshold value V_C and a comparator, the detection of the signal DATA will have as a result that the generated signal V_D will generally have a varying pulse width. This is seen in fig. 4(a) in that the pulse width t_1 is different from the pulse width t_2.

Fig. 4(b) shows an example of the detection of a data signal DATA using the technique of the invention, in which the threshold value is adjusted on the basis of the pulse width of the signal DATA. As appears from fig. 4(b), this adjustment results in a constant pulse width in the signal V_D. In fig. 4(b), the pulse width t_1 is thus equal to the pulse width t_2, which is equal to the constant pulse width in the resulting output signal V_Q.

Fig. 5 shows an example of a circuit of the invention in which a possible difference in logic voltage levels between logic signals is compensated. Fig. 5 is an extension relative to fig. 3 in that a possible difference between the logic voltage levels of the input signal V_D and the output signal V_Q from the D-flip-flop 4 in fig. 3 is

compensated. The parts of the circuit which are identical with those in fig. 3 have same reference numerals as in fig. 3.

Fig. 5 differs from fig. 3 in that the data signal DATA is fed to a comparator 16, from which both the output signal V_D and the associated inverted signal are fed to the D-flip-flop 8 so that the output signal V_D from the comparator 16 is fed to the data input on the D-flip-flop 8, while the inverted output signal from the comparator 16 is fed to the inverted data input on the D-flip-flop 8.

The output signal V_D and the associated inverted output signal from the comparator are likewise fed to a circuit 11 which generates a signal representing the temporal mean value of V_D. Correspondingly, both the output signal V_Q from the D-flip-flop 8 and the corresponding inverted output signal are fed to a circuit 12, which, like the circuit 11, generates an output signal representing the temporal mean value of V_Q. Suitable calibration causes the output signals from the circuits 11 and 12 to have signals in the same voltage ranges, so that the difference between the output signals from the circuits 11 and 12 represents the difference in pulse widths between the signals V_D and V_Q.

The output signals from the circuits 11 and 12 are fed to an integrator 19 which has the same function as the differential low-pass filter 9 in fig. 2, merely with the difference that the low-pass filtering in fig. 5 is positioned in the circuits 11 and 12 so that the circuit 19 is a pure integrator.

A possible difference in the logic voltage levels of the signals V_D and V_Q is compensated by using the circuit

shown in fig. 5, thereby ensuring that the differential temporal mean value of the signals V_D and V_Q gives correct information on the difference in the pulse width between the signals V_D and V_Q. For example, a situation in which the signals V_D and V_Q have the same temporal value will occur precisely when the pulse width of the signals V_D and V_Q are the same.

Patent Claims:

1. A method of detecting pulse-shaped data signals, wherein the data signals are compared with a reference signal, which is dependent on the data signals, to generate a detected pulse signal, characterized in that a clock signal is extracted from the detected pulse signal to generate a reference pulse signal in response to the detected pulse signal, and that the detected pulse signal and reference pulse signal are compared to generate the reference signal so that the pulse width of the detected pulse signal is adjusted to correspond to the pulse width of the reference pulse signal.

2. A method according to claim 1, characterized in that the reference signal is generated with sluggishness so that the reference signal varies slowly with respect to the frequency of the data signal.

3. A method according to claim 1 or 2, characterized in that the size of the reference signal is kept within a range positioned between and at a distance from the maximum and minimum levels of the data signal.

4. A method according to claims 1-3, characterized in that the detected pulse signal and the reference pulse signal are generated differentially.

5. A circuit for detecting pulse-shaped data signals and comprising a comparator for comparing the data signals with a reference signal so that a detected pulse signal is generated, characterized in that the circuit comprises a clock extraction circuit adapted to generate a clock signal from the detected pulse signal, and

comprises a generator circuit adapted to generate a reference pulse signal representing the detected pulse signal with a pulse width which is dependent on the clock signal period, as well as comprises a comparison circuit adapted to compare the detected pulse signal with the reference pulse signal to generate the reference signal so that the pulse width of the detected pulse signal is adjusted to correspond to the pulse width of the reference pulse signal.

6. A circuit according to claim 5, c h a r a c t e r i z e d in that the generator circuit is a D-flip-flop adapted to receive the detected pulse signal on the data input and to receive the generated clock signal on the clock input.

7. A circuit according to claims 5 or 6, c h a r a c t e r i z e d in that the comparison circuit is built as a differential amplifier whose inputs are connected to receive the detected pulse signal and the reference pulse signal, respectively.

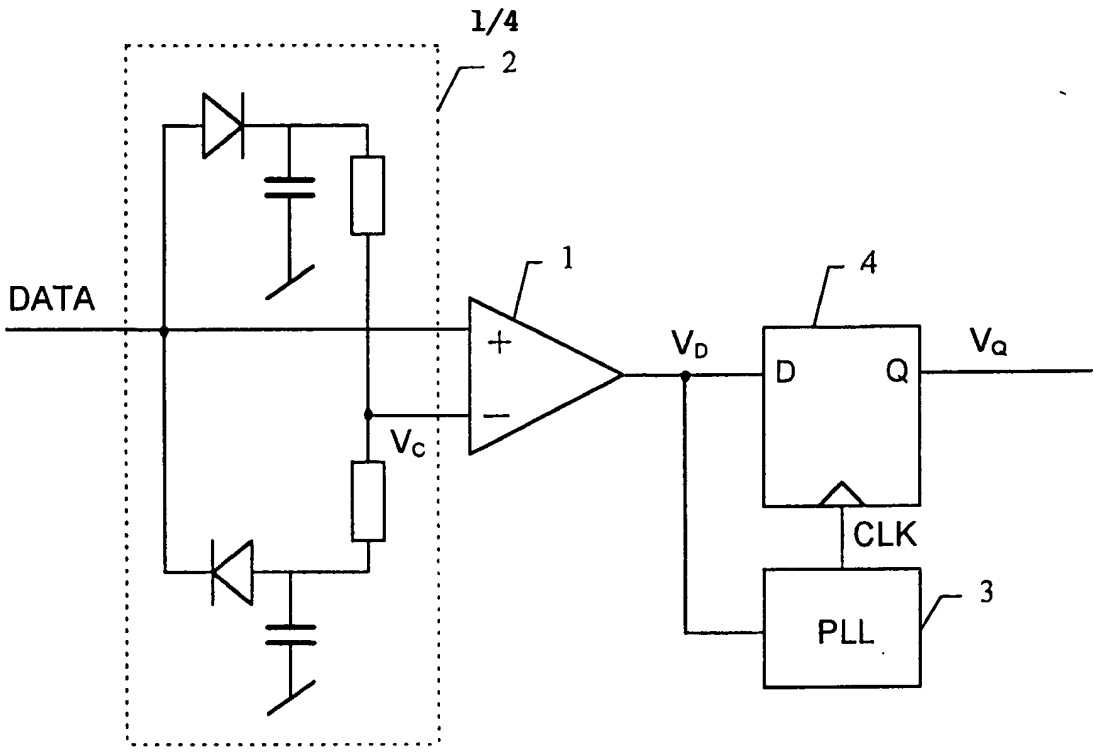
8. A circuit according to claims 5-7, c h a r a c t e r i z e d in that it comprises a low-pass filter to filter the detected pulse signal and the reference pulse signal.

9. A circuit according to claims 5-8, c h a r a c t e r i z e d in that the reference signal is connected to the input terminal of the comparator via a limiter circuit.

10. A circuit according to claims 5-9, c h a r a c t e r i z e d in that it comprises a compensation circuit adapted to compensate differences, if any, in the

logic voltage levels of the detected pulse signal and the reference pulse signal, respectively.

11. A circuit according to claim 10, c h a r a c t e r - i z e d in that the compensation circuit comprises one or more differential amplifiers whose inputs are connected to receive a differential pulse signal and whose output is connected to an input on the comparison circuit.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DATA
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4
V_D
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Q
V_Q
V_C
CLK
3
PLL

Fig. 1

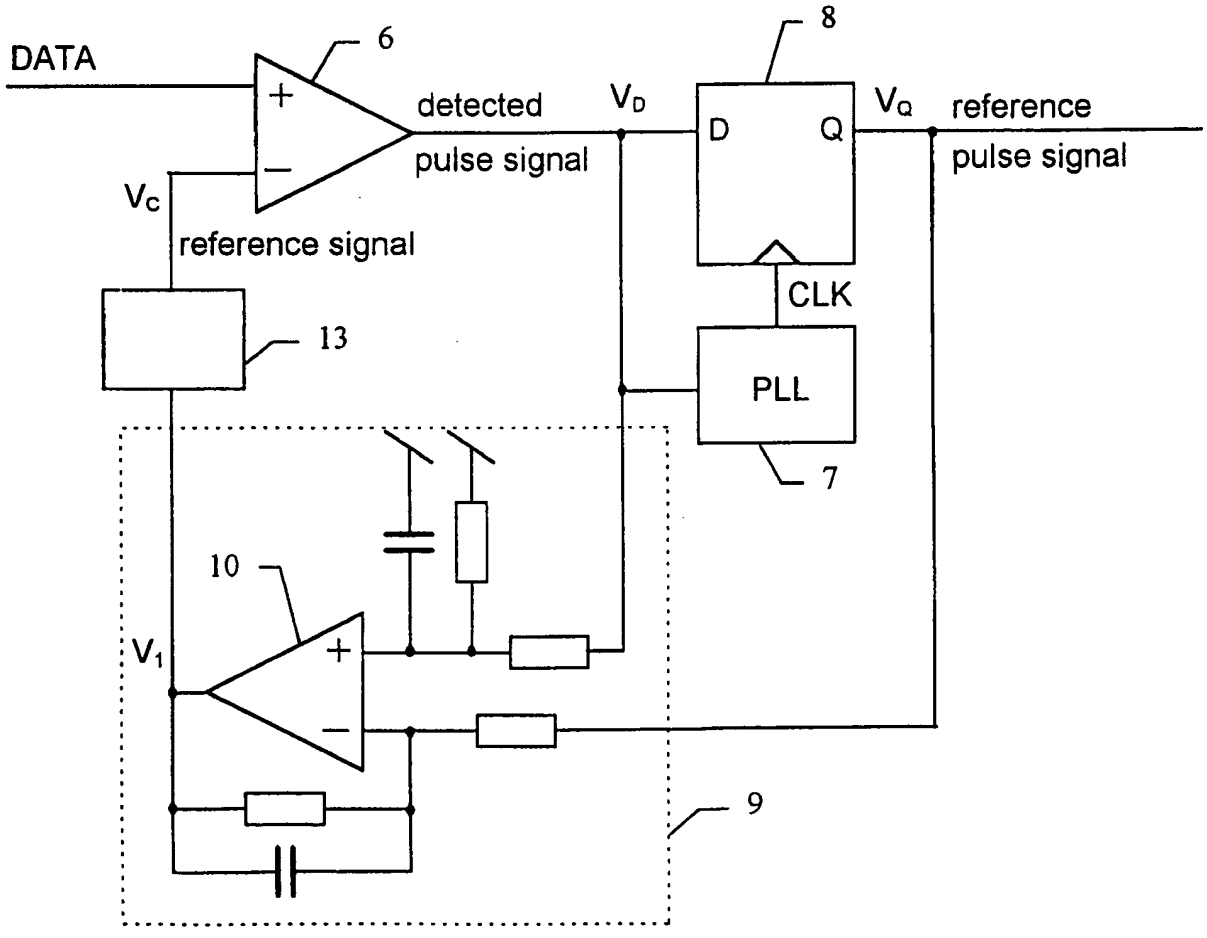

DATA
6
8
detected
pulse signal
V_D
D
Q
V_Q
reference
pulse signal
V_C
reference signal
CLK
13
PLL
7
10
V_1
9

Fig. 2

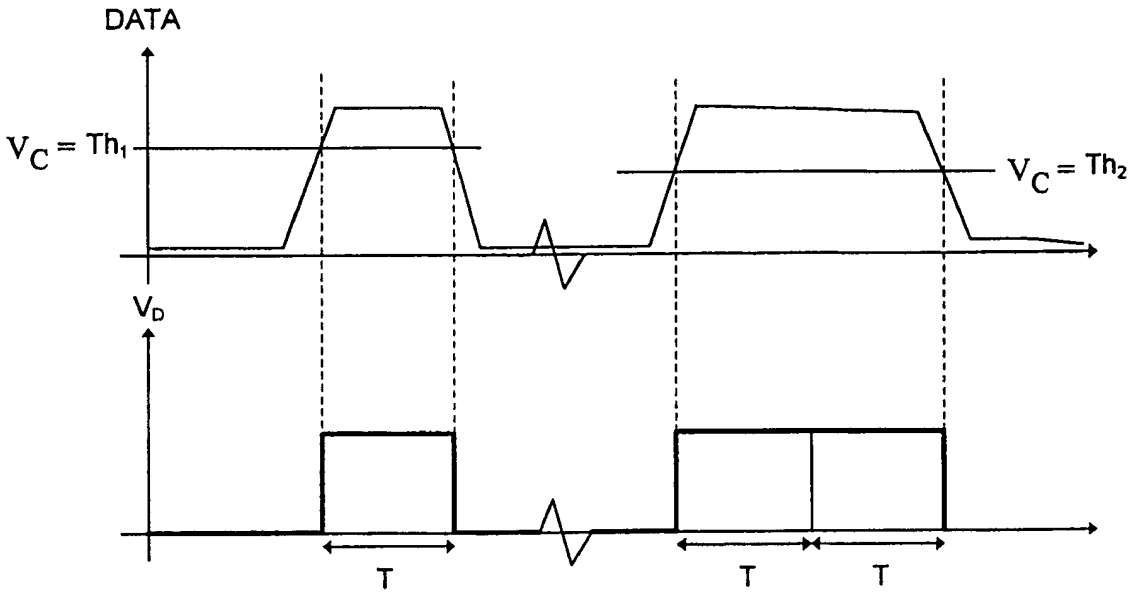
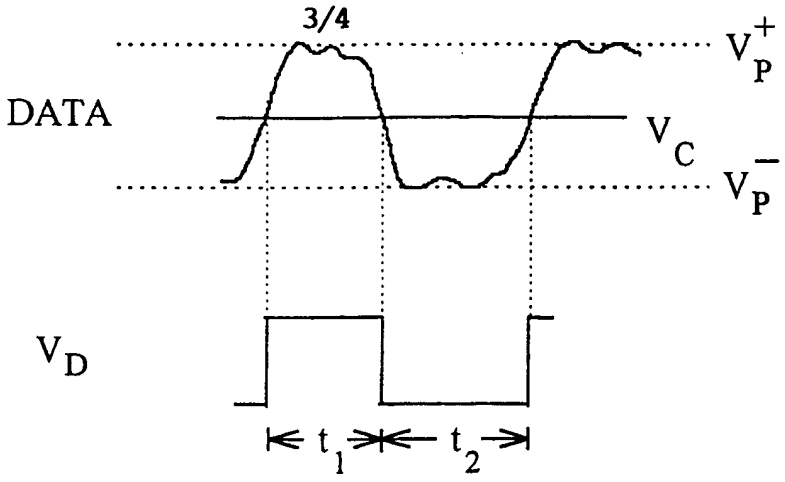
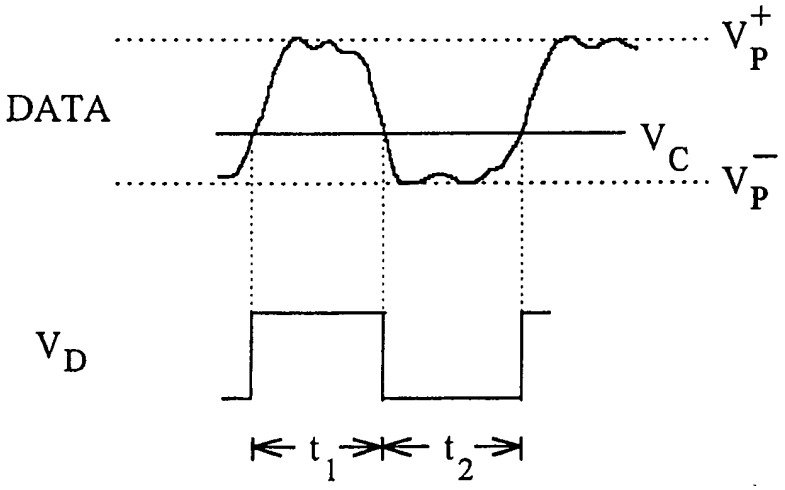


Fig. 3

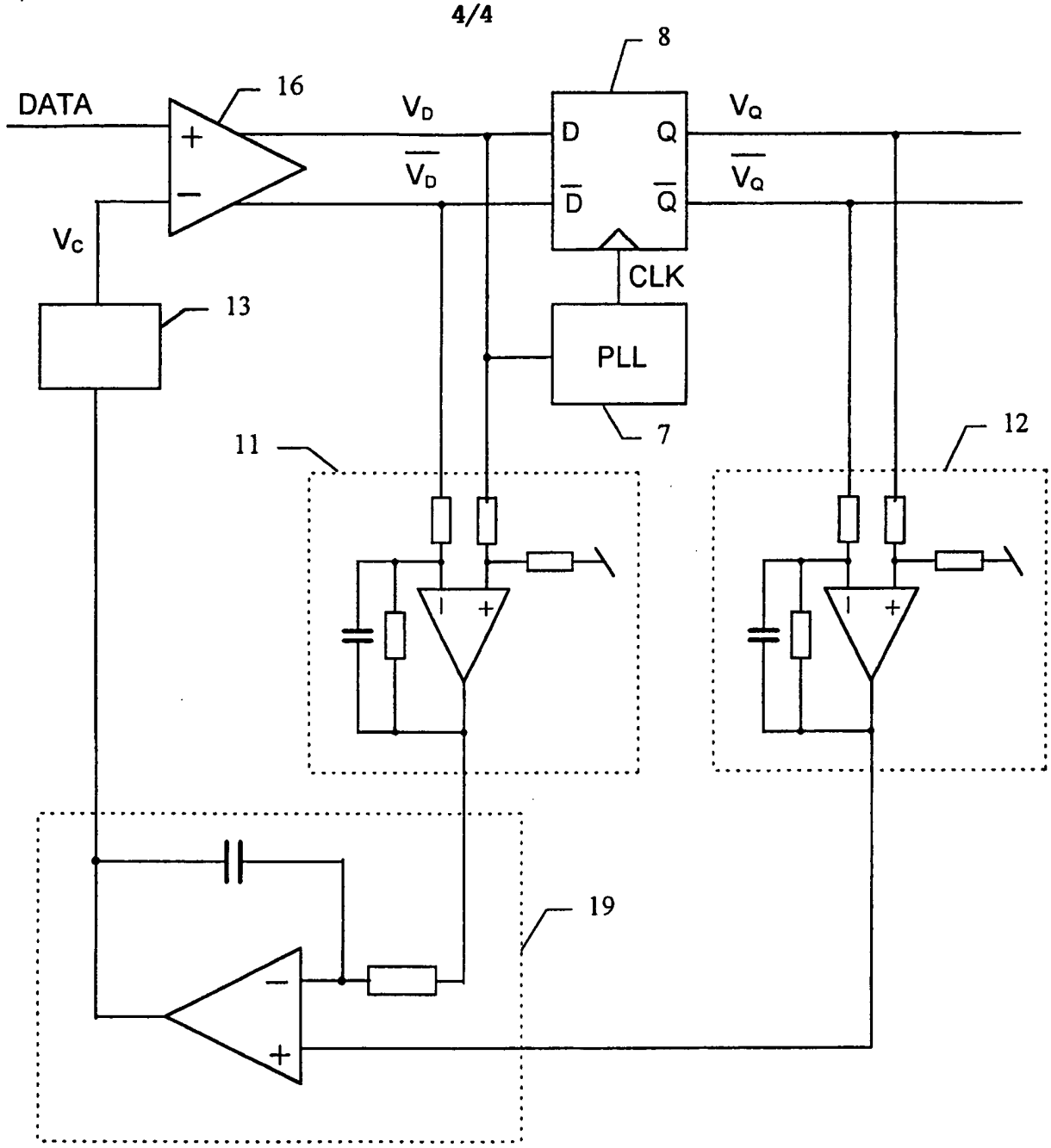


(a)



(b)

Fig. 4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DATA
16
V_D
V_Q
D
Q
$\overline{V_D}$
$\overline{V_Q}$
$\overline{D}$
$\overline{Q}$
V_C
CLK
13
PLL
7
11
12
19

Fig. 5.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/DK 97/00593

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H03K 5/04, H04Q 1/36
According to International Patent Classification (IPC) or to both national classification and IPC

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4592072 A (R.E. STEWART), 27 May 1986 (27.05.86), figures 1,2A, abstract	1,5
A	--	2-4,6-11
Y	DE 3816973 A1 (PIONEER ELECTRONIC CORP.), 22 December 1988 (22.12.88), see the whole document	1,5
A	--	2-4,6-11
A	Patent Abstracts of Japan, Vol 15,No 408, E-1123 abstract of JP 3-166815 A (NEC CORP), 18 July 1991 (18.07.91)	1-11
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12 May 1998	15 -05- 1998
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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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